2.8 A 1.2V 5.2mW 40dB 2.5Gb/s Limiting Amplifier in 0.18µm CMOS Using Negative-Impedance Compensation

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Internet access and multimedia networking has recently been proliferated and it mandates high-speed communications of a large volume of data. Thereby, optical communication systems become more attractive, even for short-distance LAN applications. The optical systems are required to provide outstanding performance in terms of bandwidth, gain, sensitivity, etc. Therefore, most commercial circuits have been implemented in GaAs, InP-based HBT, or SiGe HBT process. However, the rapid advance in deep-submicron CMOS technologies leads to the feasible implementation of high-speed front-end CMOS circuits on a single-silicon substrate with very-low supply voltages.

Typically, optical receiver systems consist of an optical detector, a a trans-impedance amplifier (TIA), a limiting amplifier (LA), and a clock and data recovery (CDR) circuit. Especially, the LA demands a number of design considerations, such as high gain to provide reliable operations of the following CDR circuit, wide bandwidth to avoid inter-symbol interference (ISI), offset cancellation, etc. Previously, gigabit CMOS LAs have been reported [1, 2, 3, 4], where well-known broadband circuit techniques have been utilized to acquire high-speed operations, including inductive peaking and capacitive degeneration. However, the inductive-peaking technique has critical drawbacks, i.e. large silicon area due to passive inductors and high supply voltage for active inductors [1, 2]. Also, reverse scaling technique in a cascade configuration was exploited to implement a 32dB 2.5Gb/s amplifier [2]. However, it required a charge-pump circuit for a gate-bias voltage higher than the 2.5V supply for active inductors. In addition, active feedback technique was employed for a 10Gb/s amplifier [3]. Yet, a number of passive inductors were utilized for shunt peaking. In this paper, an inductorless LA is realized in 0.18µm CMOS by incorporating the negative-impedance compensation technique [4]. The proposed LA achieves 2.5Gb/s operations with 40dB gain and dissipates 5.2mW from a single 1.2V supply.

Figure 2.8.1 shows the architecture of the proposed LA that consists of an input buffer with 50Ω input matching network, 4 differential amplifier cells, an offset-cancellation circuit, and an output buffer. At the input buffer, V_{TT} represents the input common-mode voltage. The optimum number (N) of cascade stages is determined to be 4 so that each gain cell provides the bandwidth of about 6GHz. Figure 2.8.2 shows the schematic diagram of a gain cell, comprising a differential-gain stage (g_{m1} and R_D), a negative-resistance stage (g_{m2}), and a negative-capacitance stage (g_{m3} and C). The negative-resistance stage is necessary to enlarge the load resistance for high gain while the negative-capacitance stage is to enhance the bandwidth. In a conventional design, either g_{m1} or R_D should be enlarged to increase the voltage gain. However, the former may increase the parasitic capacitance significantly, thus limiting the bandwidth, and the latter may degrade the gain performance due to the supply-voltage limitation. Therefore, in this work both the negative-resistance and the negative-capacitance stages are employed. Hence, it can increase the load resistance and decrease the parasitic capacitance simultaneously, thus realizing a high-gain wide-band amplifier.

According to the small signal analysis, the load resistance of each gain cell except negative-capacitance stage is given by,

$$R_L = \frac{R_D}{1 - g_{m2} R_D} \quad (1)$$

As far as g_{m2} is less than $1/R_D$ to keep the total load resistance (R_L) to be positive, the proposed gain cell can operate with a low supply voltage (1.2V in this work) and provide much-less parasitic capacitance. Otherwise, the gain cell would rather operate as a latch because of its positive pole. In the negative-capacitance stage, the equivalent output impedance is given by,

$$Z_{eq} = -\frac{1}{sC} \cdot \frac{\left[g_{m3} + s(C_{gs3} + 2C)\right]}{g_{m3}} \quad (2)$$

where the zero frequency helps to boost the gain-frequency response at around -3dB frequency and thus extend the bandwidth of the LA.

Test chips of the proposed LA are implemented in a standard 0.18µm CMOS technology with f_T of 48GHz. Figure 2.8.3 shows the chip micrograph, where the core occupies the area of $0.25 \times 0.1 mm^2$. All pads include ESD protection diodes with parasitic capacitance of 0.5pF. For facilitating the measurements, the chip is mounted on a FR-4 PCB test fixture. Figure 2.8.4 demonstrates the measured eye-diagrams for 2.5Gb/s 2^{31}-1 input PRBS at different voltage levels of $10mV_{pp}$, $100mV_{pp}$, $500mV_{pp}$, and $1V_{pp}$, respectively. Here, the output voltage level is measured to be $240mV_{pp}$ for all cases. For the frequency-response measurements, an E8364A network analyzer is utilized in the frequency range of 50MHz to 8.5GHz, where the voltage gain of 40dB and the –3dB bandwidth of 2.2GHz are obtained.

Figure 2.8.5 depicts the measured sensitivity for 2.5Gb/s 2^{31}-1 input PRBS, where the electrical sensitivity is measured to be $9.5mV_{pp}$ for the BER of 10^{-12}. Also, the overload level of the LA is measured and the BER is still below 10^{-12} for the input voltage higher than $1.2V_{pp}$.

Figure 2.8.6 demonstrates the measured rms jitter for various input signal levels and data rates. With $10mV_{pp}$ input PRBS data stream, the rms jitters for 1.25Gb/s, 2.5Gb/s, and 3.125Gb/s are measured to be $11ps_{rms}$, $21ps_{rms}$, and $23ps_{rms}$, respectively.

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References:
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[3] S. Galal and B. Razavi, "10Gb/s Limiting Amplifier and Laser/Modulator Driver in 0.18µm CMOS Technology," *ISSCC Dig. Tech. Papers*, pp. 188-189, Feb., 2003.
[4] K. Yoo, G. Han, and S. M. Park, "A 5.1mW, 2.5Gb/s Limiting Amplifier for Optical Communications," *Proc. IEEE ICECS*, Dec., 2006.

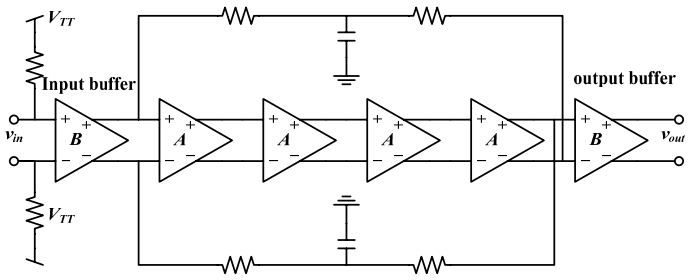

Figure 2.8.1: Limiting-amplifier block diagram.

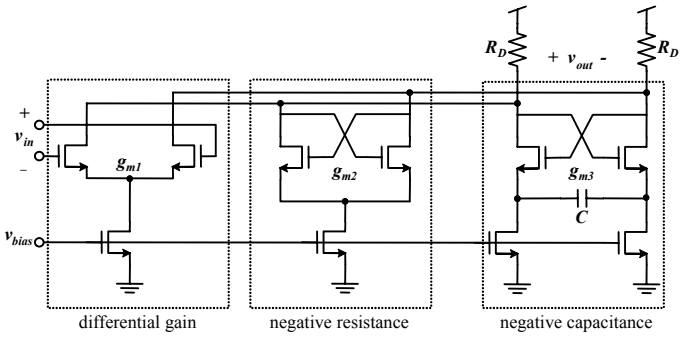

Figure 2.8.2: Schematic diagram of each gain cell.

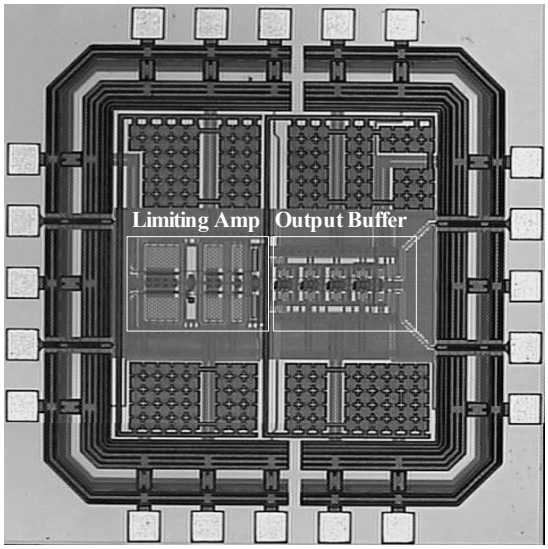

Figure 2.8.3: Chip micrograph of the LA.

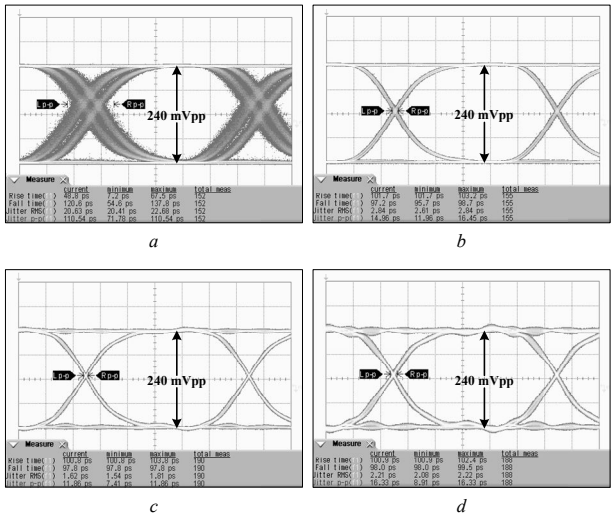

Figure 2.8.4: Measured output eye-diagrams of the LA for 2.5Gb/s PRBS with: (a) 10mV$_{pp}$, (b) 100mV$_{pp}$, (c) 500mV$_{pp}$, and (d) 1V$_{pp}$ input data. (Horizontal: 67.1ps/div, Vertical: 60mV/div).

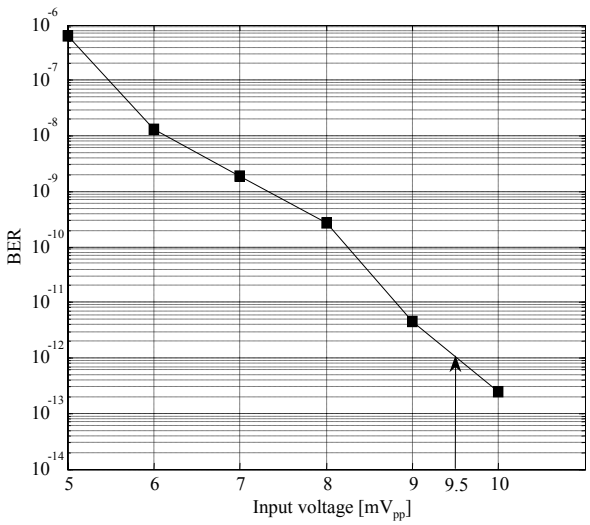

Figure 2.8.5: Measured BER and electrical sensitivity of the LA for 2.5Gb/s 2^{31}-1 PRBS.

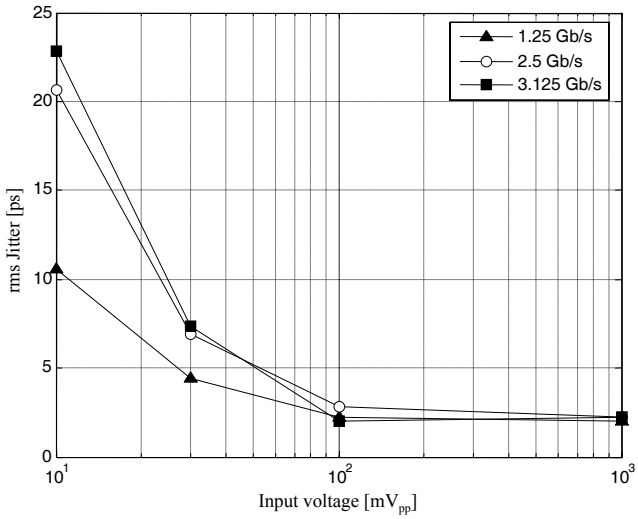

Figure 2.8.6: Measured rms jitter of the LA with variation of input voltages (10mV$_{pp}$ to 1V$_{pp}$).